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MODEL WDG-SIO

USER MANUAL

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Chapter 1: Introduction

This multifunction card contains a Watchdog Timer, an RS422/485 Serial Communications port, and an internal Temperature Alarm. There are five standard catalog options which may be installed on your card if it was ordered with these options. These are:

Option S01:   A relay is provided on the Watchdog Timer output.
Option S02:   Tranzorbs are added in the serial communications port
Option S03:   An additional connector, J1 is provided for outputs of two 16-bit counter/timers.
Option S04:   The counter/timer outputs are provided as in Option S03 plus tranzorbs are added in those I/O lines.
Option S05:   This option is mutually exclusive with Option S04 and provides relay outputs at connector J1.

The WDG-SIO is a full-length card that installs in "long" expansion slots of IBM PC/XT/AT and compatible computers. The following paragraphs describe functions provided by the WDG-SIO card.

Watchdog

It's a fact of life that computers can fail. If a computer fails it can cause catastrophic damage. There are two methods to reduce risk of computer failure; (a) redundancy and (b) a watchdog circuit. Neither method offers 100% assurance but both of these methods reduce risk or consequences of failure. Redundancy, a duplication of computer circuitry, is very expensive. On the other hand, the Watchdog card offers excellent protection from temporary malfunctions at very low cost.

An application program must communicate with the watchdog circuit at prescribed intervals. If this communication ("prompt") is missed, the Watchdog will initiate a computer reset. This restarts the computer from the beginning of the program. If the failure was temporary, proper operation is resumed. If, however, the failure is persistent, the Watchdog will continuously reset the computer. The more frequently the computer is prompted (and shorter Watchdog time selected), the less time a faulty computer has to cause damage.

The method used by the WDG-SIO card to determine loss of computer function is as follows:

a.   A counter/timer has a number greater than zero set into it by your application program.
b.   This counter/timer counts down toward zero at a 225 Hz rate.
c.   As long as the computer is functioning properly, the number in the counter/timer is periodically re-entered by your application program before the counter/timer reaches zero.
d.   If this software resetting of the timer/counter fails to occur, the timer/counter reaches zero and a hardware reset of the computer is attempted.

Implementation of this watchdog procedure can be accomplished by your application program, by AUTOEXEC.BAT, or by other appropriate software.

A type 8254 counter/timer chip is used in the Watchdog circuit. The clock source for this chip is 225 HZ derived from a crystal oscillator on the card and is independent of the computer clock. The watchdog time-out is software programmable from 5 mSec to 291 seconds.

At power turn-on, the counter/timer output should be disabled via SIO OUT1 until all devices are initialized. At the very end of initialization, SIO OUT1 (Output 1 of the Asynchronous Communication Element) should be programmed low to enable the Watchdog circuit.

The address for the Watchdog circuit is completely independent of the Serial Communication address. It is jumper selectable anywhere within the I/O address range 000 to 3FF hex.

The output of the Watchdog circuit is an open-collector transistor output rated at up to 100 mA. That output is available at terminal 1 of terminal board TB2. Terminal 2 at TB2 provides a ground return. If an inverted output is desired, you may cut the clad at jumper G and install a wire short at location H. (G and H are located immediately to the left of IC U16.)

If your card includes Option S01, then a relay output is provided at terminal board TB1. Terminal 1 connects to the normally-closed contact which is returned to ground through the relay center arm. Terminal 3 is connected to the normally-open contact until the relay is activated by a time-out at which time it is connected to ground by the relay center arm.

Counter/Timer

The 8254 counter/timer chip contains three 16-bit counters. Counter/timer 2 is used by the Watchdog circuit. If your card has Option S03, then you have access to counter/timers 0 and 1 via a 9-pin I/O connector at the rear of the computer. On-board clock frequencies of 1.843 MHz, 230 KHz, 28.8 KHz, 3.6 KHz, and 225 Hz are available by DIP switch selection. Counter/timer gate inputs and counter/timer outputs are via pins on the I/O connector.

If Option S03 was specified when your card was purchased, outputs of Counter/timers 0 and 1 are buffered by drivers capable of 120 mA drive and are available at pins 1 and 6 respectively of the 9-pin connector. If Option S04 was specified, those outputs are opto-isolated and available at pins 2 and 4. If Option S05 was specified, then relays are installed instead of opto-isolators. Relay K3 actuates on Counter/timer 0 and K2 operates on Counter/timer 1 outputs. When a relay actuates, the normally-open contacts at I/O connector pins 5 and 4 respectively are closed to pin 2 of the 9-pin I/O connector.

Temperature Alarm

The WDG-SIO card also contains a temperature alarm circuit that activates if the internal temperature in the computer becomes excessive. That alarm can initiate an interrupt so that an early shutdown may be accomplished. The Temperature Alarm circuit operates on the principle of a PN junction voltage decrease of 2.3 mV/ °C. of ambient temperature increase. The voltage across five serially-connected PN junctions is compared with a preset DC level from a potentiometer. The output of the comparator circuit can be applied, via jumper, to Interrupt outputs and/or can be read on bit 0 of the Temperature Alarm register at Watchdog base address + 4.

The potentiometer is factory set at 50 °C. If you desire to set the alarm at some other temperature, subtract the ambient temperature from the desired alarm temperature and multiply the difference by 5 X 2.3 mV. Then measure the voltage between pin 4 (-) and pin 5 (+) of U17 and adjust potentiometer RP1 for that calculated value.

Serial Interface

The Serial Interface function of the WDG-SIO card can be used for either RS422 serial communications or RS485 communications. (The RS485 specification allows multiple transmitters and receivers to communicate over a two-wire "party line" bus.) Opto-isolators are incorporated on this card to provide common-mode voltage isolation on the Tx, Rx, RTS, and CTS communications lines.

Type NS16550 UARTs are used as the Asynchronous Communication Element (ACE). Use of the same ACE as used in IBM original equipment makes the card 100 percent compatible with existing programs when the base address is set as either COM1 or COM2. However, use of the Serial Interface is not restricted to COM1 or COM2 only. Different addresses can be selected anywhere within the I/O address range 100-3FF hex.

An on-board crystal oscillator permits precise selection of baud rate from 50 to 56000.

The output transceiver used, the new generation type 75176, is capable of driving extremely long communication lines at high baud rates. It can drive 60 mA on balanced lines and can receive input signals as low as 200 mV amplitude superimposed on common mode noise of maximum -7V/+12V. In case of communication conflict, the transceivers feature thermal shutdown.

The communication lines are loaded at the receiver and biased at the transmitter. Also, an on-board DC-DC converter provides isolated power to the transceiver and opto-isolators are provided in the serial I/O lines.

Two LED indicators are provided in the Serial Interface circuit. These LEDs blink to indicate activity on the transmitting and receiving lines and are useful for problem diagnosis.

In addition to dual, differential Transmit and Receive lines, single-ended, buffered RTS and CTS lines are provided on the I/O connector. The RTS line can be used to control the Transmitter and Receiver. The CTS line can be used to check for proper installation of the communication cable. To check for proper cable connection, introduce +5VDC to the CTS line on the cable side of the connector. Then read the CTS bit by software. Signal ground and +5 VDC are available at the I/O connector.

Full-Duplex, Half-Duplex, or Simplex configuration can be selected by jumper options.

Utility Software

Utility software is provided on CD with the WDG-SIO card. This software includes a base address locator program to help you select base addresses for the Watchdog and the Serial I/O port plus an illustrated setup program to help you set switches and jumpers according to how you wish to use the card. Also, software drivers and sample programs for use with QuickBASIC, C, and Pascal are included.

Specification

Watchdog Timer
- Time-out: Software selectable from 5 mSec to 291 Sec in 5 mSec increments.
- Output Pulse Width: 4 msec.
- Clock: 225 Hz, crystal controlled.
- Address: Continuously mappable within 000 to 3FF hex I/O range.
- Relay Option: Contacts rated at 250 mA at up to 24VDC.

Temperature Alarm
- Level: Factory preset at 50 °C. ±2 °C. Adjustable.
- Interrupt Output: Jumper selectable.
- Alternate Output: Can be read from bit 0 at base address + 4.

Serial Interface
- Multipoint: Compatible with RS422 and RS485 specifications.
- Common Mode Voltage: -7V to +12V CMV will not affect operation.
- Driver Output Capability: 60 mA maximum.
- Receiver Input Sensitivity: Can detect signals as small as +/-200 mV.
- Baud Rate: 50 to 9600 baud. (to 56,000 baud optional). Crystal oscillator on board.
- Address: Continuously mappable within I/O address range 000-3FF hex.

Counter Output Option (Counters 0 and 1)
- Standard Output: Open collector transistor, 100 mA.
- Opto-Isolated Output Option: 2 mA at up to 24VDC.
- Relay Output Option: Contacts rated at 250 mA at up to 24VDC.

Environmental
- Operating Temperature Range: 0 °C. to +60 °C.
- Storage Temperature Range: -50 °C. to +120 °C.
- Humidity: 10% to 90% RH, non-condensing.

- Power Required: +5 VDC at 420 mA typical, 500 mA maximum.
- Size: 13.3 inches long. Requires full size slot.

Figure 1-1: WDG-SIO Block Diagram

Chapter 2: Installation

The software provided with this card is contained on either one CD or multiple diskettes and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your software format and operating system. Substitute the appropriate drive letter for your CD-ROM or disk drive where you see d: or a: respectively in the examples below.

CD Installation

DOS/WIN3.x
1. Place the CD into your CD-ROM drive.
2. Type d:K to change the active drive to the CD-ROM drive.
3. Type installK to run the install program.
4. Follow the on-screen prompts to install the software for this card.

WIN95/98/NT
a. Place the CD into your CD-ROM drive.
b. The CD should automatically run the install program after 30 seconds. If the install program does not run, click START | RUN and type d:install, click OK or press K.
c. Follow the on-screen prompts to install the software for this card.

3.5-Inch Diskette Installation

As with any software package, you should make backup copies for everyday use and store your original master diskettes in a safe location. The easiest way to make a backup copy is to use the DOS DISKCOPY utility.

In a single-drive system, the command is:

diskcopy a: a:K

You will need to swap disks as requested by the system.
In a two-disk system, the command is:

diskcopy a: b:K

This will copy the contents of the master disk in drive A to the backup disk in drive B.

To copy the files on the master diskette to your hard disk, perform the following steps.
1.   Place the master diskette into a floppy drive.
2.   Change the active drive to the drive that has the diskette installed. For example, if the diskette is in drive A, type a:K.
3.   Type installK and follow the on-screen prompts.

Directories Created on the Hard Disk

The installation process will create several directories on your hard disk. If you accept the installation defaults, the following structure will exist.

[CARDNAME]
Root or base directory containing the SETUP.EXE setup program used to help you configure jumpers and calibrate the card.

DOS\PSAMPLES: A subdirectory of [CARDNAME] that contains Pascal samples.
DOS\CSAMPLES: A subdirectory of [CARDNAME] that contains "C" samples.
Win32\language: Subdirectories containing samples for Win95/98 and NT.

WinRisc.exe
A Windows dumb-terminal type communication program designed for RS422/485 operation. Used primarily with Remote Data Acquisition Pods and our RS422/485 serial communication product line. Can be used to say hello to an installed modem.

ACCES32
This directory contains the Windows 95/98/NT driver used to provide access to the hardware registers when writing 32-bit Windows software. Several samples are provided in a variety of languages to demonstrate how to use this driver. The DLL provides four functions (InPortB, OutPortB, InPort, and OutPort) to access the hardware.

This directory also contains the device driver for Windows NT, ACCESNT.SYS. This device driver provides register-level hardware access in Windows NT. Two methods of using the driver are available, through ACCES32.DLL (recommended) and through the DeviceIOControl handles provided by ACCESNT.SYS (slightly faster).

SAMPLES

Samples for using ACCES32.DLL are provided in this directory. Using this DLL not only makes the hardware programming easier (MUCH easier), but also one source file can be used for both Windows 95/98 and WindowsNT. One executable can run under both operating systems and still have full access to the hardware registers. The DLL is used exactly like any other DLL, so it is compatible with any language capable of using 32-bit DLLs. Consult the manuals provided with your language's compiler for information on using DLLs in your specific environment.

VBACCES

This directory contains sixteen-bit DLL drivers for use with VisualBASIC 3.0 and Windows 3.1 only. These drivers provide four functions, similar to the ACCES32.DLL. However, this DLL is only compatible with 16-bit executables. Migration from 16-bit to 32-bit is simplified because of the similarity between VBACCES and ACCES32.

PCI

This directory contains PCI-bus specific programs and information. If you are not using a PCI card, this directory will not be installed.

SOURCE

A utility program is provided with source code you can use to determine allocated resources at run-time from your own programs in DOS.

PCIFind.exe

A utility for DOS and Windows to determine what base addresses and IRQs are allocated to installed PCI cards. This program runs two versions, depending on the operating system. Windows 95/98/NT displays a GUI interface, and modifies the registry. When run from DOS or Windows3.x, a text interface is used. For information about the format of the registry key, consult the card-specific samples provided with the hardware. In Windows NT, NTioPCI.SYS runs each time the computer is booted, thereby refreshing the registry as PCI hardware is added or removed. In Windows 95/98/NT PCIFind.EXE places itself in the boot-sequence of the OS to refresh the registry on each power-up.

This program also provides some COM configuration when used with PCI COM ports. Specifically, it will configure compatible COM cards for IRQ sharing and multiple port issues.

WIN32IRQ

This directory provides a generic interface for IRQ handling in Windows 95/98/NT. Source code is provided for the driver, greatly simplifying the creation of custom drivers for specific needs. Samples are provided to demonstrate the use of the generic driver. Note that the use of IRQs in near-real-time data acquisition programs requires multi-threaded application programming techniques and must be considered an intermediate to advanced programming topic. Delphi, C++ Builder, and Visual C++ samples are provided.

Findbase.exe

DOS utility to determine an available base address for ISA bus , non-Plug-n-Play cards. Run this program once, before the hardware is installed in the computer, to determine an available address to give the card. Once the address has been determined, run the setup program provided with the hardware to see instructions on setting the address switch and various option selections.

Poly.exe

A generic utility to convert a table of data into an nth order polynomial. Useful for calculating linearization polynomial coefficients for thermocouples and other non-linear sensors.

Risc.bat

A batch file demonstrating the command line parameters of RISCTerm.exe.

RISCTerm.exe

A dumb-terminal type communication program designed for RS422/485 operation. Used primarily with Remote Data Acquisition Pods and our RS422/485 serial communication product line. Can be used to say hello to an installed modem. RISCTerm stands for Really Incredibly Simple Communications TERMinal.

Installing the Card

Before installing the WDG-SIO card, carefully read the Option Selection and Address Selection chapters of this manual and configure the card according to your requirements. Be especially careful with Address Selection. If the address of two installed functions overlap, you will experience unpredictable computer behavior.

To Install the Card

1.   Remove power from the computer.
2.   Remove the computer cover.
3.   Remove the blank I/O backplate.
4.   Install jumpers for selected options. See Option Selection.
5.   Select base addresses for the Serial Interface and for the Watchdog and Temperature Alarm functions. See Address Selection.
6.   Install the card in an I/O expansion slot. Make sure that the card mounting bracket is properly screwed into place and that there is a positive chassis ground.
7.   Install the "Reset" wire from TB1-1 to the "Power Good" signal on the power supply connector J8, pin 1 using the clamp provided or to the active terminal of the Reset switch.

8.   After inserting the power-good line into the clamp, compress the metal bar with pliers and close the protective cover.

POWER GOOD LINE,
PIN ONE (1),
USUALLY ORANGE

To WATCHDOG TERMINAL BLOCK

P8

P9
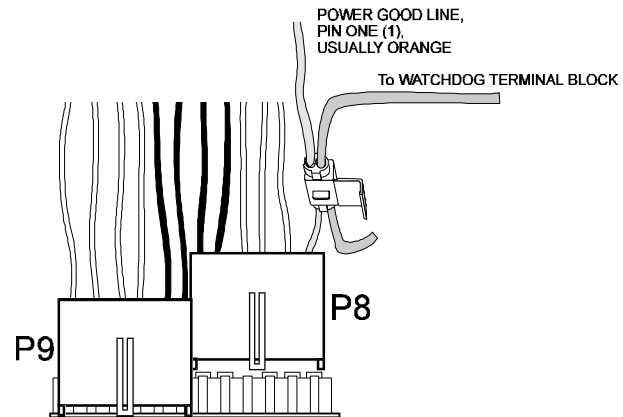
9.   Plug in the RS422/485 communications connector and secure it with the mounting screws.
10.   Inspect for proper fit of the card and connectors and tighten screws.
11.   Turn the computer ON and observe the LEDs on the card. The LEDs will blink when there is activity on the communication line.
12.   If everything checks good, replace the computer cover.

To ensure that there is minimum susceptibility to EMI and minimum radiation, it is important that there be a positive chassis ground. Also, proper EMI cabling techniques (cable connect to chassis ground at the I/O connector, twisted-pair wiring, and, in extreme cases, ferrite level of EMI protection) must be used for input/output wiring.

CE-marked versions of WDG-SIO meet the requirements of EN50081-1:1992 (Emissions), EN50082-1:1992 (Immunity), and EN60950:1992 (Safety).

Chapter 3: Option Selection

Refer to Figure 1-1, WDG-SIO Block Diagram and the Option Selection Map when reading this section of the manual. Card operation is determined by jumper installation as described in the following paragraphs.

Serial I/O Port

CTS Control

Serial communications will not operate without this signal. The function of the CTS jumper is to provide the signal when it is not externally supplied. If you prefer, you can omit this jumper and install a jumper between CTS (pin 5) and +5VDC (pin 9) on the mating D connector P1. This jumper in the mating connector provides a handy diagnostic tool because the card will not operate unless the mating connector is properly installed.

Termination and Bias

A transmission line should be terminated at the receiving end in its characteristic impedance. Installing a jumper at the location labeled LD applies a 136Ω load across the input for RS422 mode and across the transmit/receive input/output for RS485 operation. When noise is a potential problem on long lines, the terminating resistance should be divided and its center point grounded to help reduce noise voltage pickup. To accomplish this, also install a jumper at the position marked LD GND for 68-ohm termination resistance on the positive and negative branches of the receiving line.

Simplified Schematic

In RS485 mode, where there are multiple terminals, only the RS485 ports at each end of the network should have terminating resistors as described above. If the card is to have an ungrounded load, do as above except do not install the LD GND jumper. (See Appendix A, Application Considerations.) Also, for RS485 operation, there must be a bias on the RX+ and RX- lines. If this card is to provide the bias, install jumpers at the locations labeled +BIAS and -BIAS.

RTS Control

For RS485 operation, installing a jumper at the location marked RTS (adjacent to transformer T1) allows the state of the RTS line to be controlled by the UART. Without this jumper, the RTS signal will always be high and allow the port to start a transmission at any time.
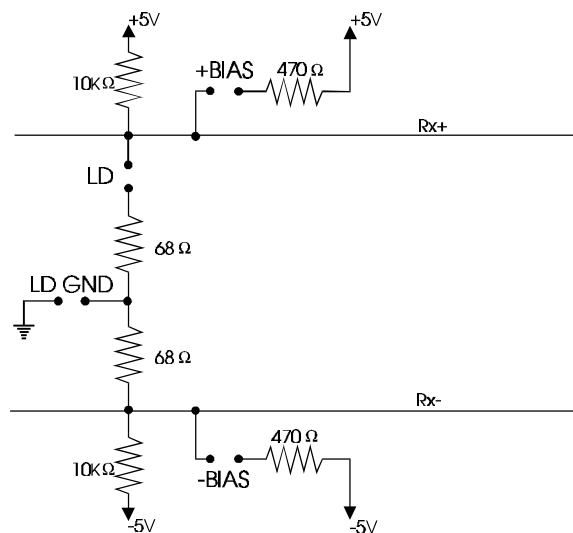
Simplex or Duplex

The receiver can be set in either Simplex or Duplex by installing jumpers marked SX or DX respectively. Simplex mode is intended for one-way communication; either transmit or receive. Duplex mode allows transmission or reception either simultaneous or alternatively. In the Duplex mode, the receiver is always enabled and the echo of the port's transmission is fed back to the UART receiver. In the Simplex mode, the receiver is enabled if RTS is low.

Connections for Simplex (transmit only or receive only) are:

    Receive: DX and FDX jumpers, connector pins 12 and 13.
    Transmit: SX and FDX jumpers, connector pins 24 and 25.

Full or Half-Duplex

Either Full or Half-Duplex can be selected by installing jumpers at the locations marked FDX or HDX respectively. Full-Duplex allows simultaneous bi-directional communications and is selected by installing the FDX jumper. Half-Duplex allows bi-directional transmitter and receiver operation but only one at a time. Proper selection depends on the wire connections used to connect the two serial ports.

RS422 operation requires a jumper at FDX and RS485 operation requires a jumper at HDX.

Connections for Half-Duplex (transmit and receive taking turns) and Full-Duplex (transmit and receive at the same time) are as follows:

Mode		Jumpers	Card A	Card B
Half-Duplex	2-wire with local echo	DX-HDX-RTS	12	13
			13	12
Half-Duplex	2-wire without local echo	SX-HDX-RTS	12	13
			13	12
Full-Duplex	4-wire without local echo	DX-FDX	12	13
			13	12
			24	25
			25	24

Watchdog Output

If an inverted output from the watchdog circuit (i.e., held high) is desired, you may cut the clad at jumper location "G" and install a wire short at location "H". (G and H are located immediately to the left of IC U16.)

The Watchdog circuit can be disabled by installing a jumper at the location marked WDOG OFF.

Counter/Timer Clock Frequency

The clock frequency applied to counter/timers 0 and 1 can be selected by DIP switches S4 and S3 respectively. You can select 28.8, 3.6, 230, 225, or 1843 Hz.

Interrupts

Interrupts coming from the Temperature Alarm circuit and/or the Serial Interface are enabled by installing jumpers at locations marked IRQ2, 3, 4, 5, 6, 7, 10, 11, 12, 14, and 15. Temperature Alarm interrupts are selected at the jumper block labeled TMP. Serial Communication interrupts are selected at the adjacent jumper block labeled COM. (Note: Levels 10, 11, 12, 14, and 15 apply only for AT-Bus applications.)
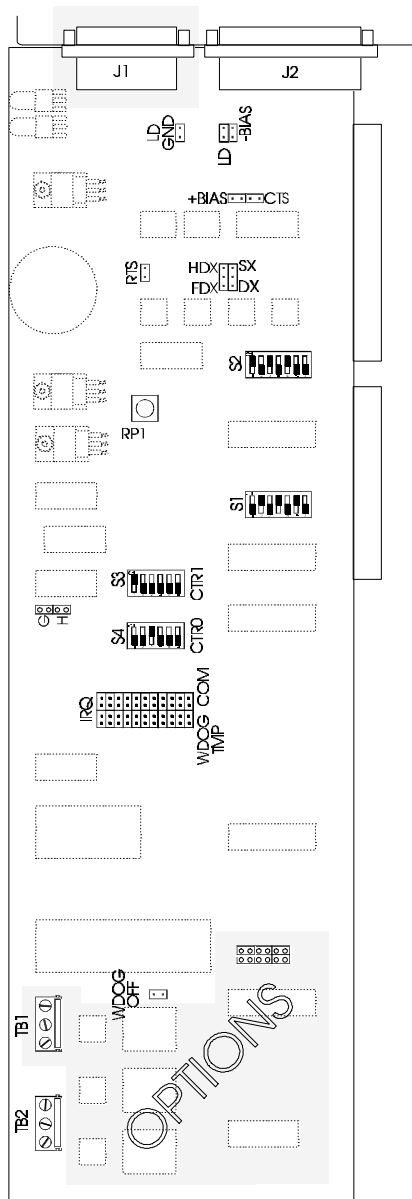
Switches:

S1=Serial Port Base Address
S2=Watchdog Base Address
S3=Counter 1 clock input select
S4=Counter 2 clock input select

Jumpers:

LD GND = Load Ground Select
LD = Load Select
+BIAS = +Bias Select
-BIAS = -Bias Select
CTS = Clear-To-Send Signal Control Select
RTS = Ready-To-Send Signal Control Select
HDX/FDX = Half-/Full-Duplex Select
SX/DX = Simplex/Duplex Select
IRQ-WDOG TMP = Watchdog Function IRQ Select
IRQ-COM = Serial Port IRQ Select
WDOG OFF = Watchdog Function Disable Jumper

Connectors:

J1 = Optional CTR 0 & CTR 1 & Watchdog Relay
        output connector
J2 = Serial port and Watchdog Function Connector
TB1 = Optional Watchdog Relay Output Connector
TB2 = Watchdog Function Connector

Shorts Positions:

G & H: Invert/non-invert Watchdog
            output select

Figure 3-1: WDG-SIO Option Selection Map

Chapter 4: Address Selection

The card provides separate base address capabilities for the Serial Interface and for the Watchdog and Temperature Alarm. The Serial Interface requires eight bytes of address space and the Watchdog and Temperature Alarm require an additional five bytes. Accordingly, base addresses for these functions are separated and selected at separate DIP switches labeled COM and WDOG-TMP respectively. (See the Option Selection Map on the previous page.) The FINDBASE program supplied will assist you in selecting addresses that will avoid conflict.

Switches are marked A3 through A9. The DIP switch that sets the base address of the Serial Interface is located to the right of U1 and the DIP Switch for the Watch dog and Temperature Alarm is located to the right of U2.

The base addresses can be selected anywhere within the I/O address range 100-3FF (except 1F0 through 1F8) for ATs and 200-3FF for XTs, provided that they do not overlap with other functions. If in doubt, refer to the table on the following page for a list of standard address assignments.

Hex Range	Usage
000-01F	DMA Controller 1
020-03F	INT Controller 1, Master
040-05F	Timer
060-06F	8042 (Keyboard)
070-07F	Real Time Clock, NMI Mask
080-09F	DMA Page Register
0A0-0BF	INT Controller 2
0C0-0DF	DMA Controller 2
0F0	Clear Math Coprocessor Busy
0F1	Reset Coprocessor
0F8-0FF	Arithmetic Processor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Asynchronous Comm'n (Secondary)
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC or Binary Synchronous Comm'n 2
3A0-3AF	Binary Synchronous Comm'n 1
3B0-3BF	Monochrome Display/Printer
3C0-3CE	Local Area Network
3D0-3DF	Color/Graphic Monitor
3F0-3F7	Floppy Diskette Controller
3F8-3FF	Asynchronous Comm'n (Primary)

Table 4-1: Standard Address Assignments for 286/386/486 Computers

Address Setup switch locations are marked A3 through A9. In order to configure the desired address, assign "1" to the OFF position of these switches and assign "0" to the ON position of these switches. These 1's and 0's are a binary representation of the base address. This binary number is then converted to a hexadecimal number.

Switch Label	A9	A8	A7	A6	A5	A4	A3
Addr Line	A9	A8	A7	A6	A5	A4	A3

For example, as illustrated below, jumper selection corresponds to binary 10 1101 1xxx (or hex 2D8). The "xxx" represents address lines A2, A1, and A0 used on the card to select individual registers as described in Chapter 5, Programming of this manual.

Switch Label	A9	A8	A7	A6	A5	A4	A3
Jumper Installed	no	yes	no	no	yes	no	no
Binary Representation	1	0	1	1	0	1	1
Conversion Factors	2	1	8	4	2	1	8
Hex Representation	2			D			8

Review the Address Selection Table carefully before selecting the card address. If the addresses of two installed functions overlap you will experience unpredictable computer behavior.

Chapter 5: Programming

This section of the manual is divided into two parts; programming for the Watchdog and Temperature Alarm functions, and programming for the Serial Interface function. The program examples provided are intended as a guide rather than working software. ACCES assumes no liability for their use.

Watchdog

The Watchdog and Temperature Alarm functions of the WDG-SIO card use five consecutive addresses in I/O space as listed in the following table.

Address	Read	Write
Base Address	Read Counter 0	Load Counter 0
Base Address +1	Read Counter 1	Load Counter 1
Base Address +2	Read Counter 2	Load Counter 2
Base Address +3	Unused	Load Control Reg'st
Base Address +4	Read Temp Alarm	Illegal

Table 5-1: I/O Address Map

The Watchdog function includes an eight-bit control register at base address + 3. That control register allows software selection and/or control of the function. The format of this register and bit functions are as follows:

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Functions of the bits are as follows:

SC1 and SC0

These bits are used to select counter/timers 0, 1, or 2. SC1 is the most significant bit. (Note: If your card contains Option C, you have access to counter/timers 0 and 1.) The code assignment for bits SC1 and SC0 is:

00 = Select Counter/Timer 0   10 = Select Counter/Timer 2
01 = Select Counter/Timer 1   11 = Read Back Command

RL1 and RL0

These bits control reading and loading of the Counter/Timer selected by SC1 and SC0. RL1 is the most significant bit and code assignment is:

00 = Counter Latch Command
01 = Read/Load Least Significant Byte Only
10 = Read/Load Most Significant Byte Only
11 = Read/Load Least and Then Most Significant Byte

BCD

This bit commands counting modulus; 0= binary, 1= BCD.

M2, M1, and M0

These bits control the operating mode of the Counter/Timer selected by SC1 and SC0. Bit assignments and mode commanded are as follows:

M2	M1	M0	Mode
0	0	0	Mode 0: Pulse on Term'l Count
0	0	1	Mode 1: Retrig'ble One-Shot
X	1	0	Mode 2: Rate Generator
X	1	1	Mode 3: Square Wave Generator
1	0	0	Mode 4: Software Trig'd Strobe
1	0	1	Mode 5: Hardware Trig'd strobe

Modes of operation of the type 8254 Counter/Timer chip are described in the following paragraphs to familiarize you with the versatility and power of this device. The following definitions apply for use in describing operation of the 8254:

Clock: A positive pulse into the counter's clock input.
Trigger: A rising edge input to the counter's gate input.
Counter Loading: Programming of a binary count into the counter.

Mode 0: Pulse on Terminal Count

After the counter is loaded, the output is set low and will remain low until the counter decrements to zero. The output then goes high and remains high until a new count is loaded into the counter. A trigger enables the counter to start decrementing. This mode is commonly used for event counting with Counter #0.

Mode 1: Retriggerable One-Shot

The output goes low on the clock pulse following a trigger to begin the one-shot pulse and goes high when the counter reaches zero. Additional triggers result in reloading the count and starting the cycle over. If a trigger occurs before the counter decrements to zero, a new count is loaded. Thus, this forms a re-triggerable one-shot. In mode 1, a low output pulse is provided with a period equal to the counter count-down time.

Mode 2: Rate Generator

This mode provides a divide-by-N capability where N is the count loaded into the counter. When triggered, the counter output goes low for one clock period after N counts, reloads the initial count, and the cycle starts over. This mode is periodic, the same sequence is repeated indefinitely until the gate input is brought low.

Mode 3: Square Wave Generator

This mode operates periodically like mode 2. The output is high for half of the count and low for the other half. If the count is even, then the output is a symmetrical square wave. If the count is odd, then the output is high for $(N+1)/2$ counts and low for $(N-1)/2$ counts. Periodic triggering or frequency synthesis are two possible applications for this mode.

Mode 4: Software Triggered Strobe

This mode sets the output high and, when the count is loaded, the counter begins to count down. When the counter reaches zero, the output will go low for one input period. The counter must be reloaded to repeat the cycle. A low gate input will inhibit the counter.

Mode 5: Hardware Triggered Strobe

In this mode, the counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of the trigger.

In order to program the Watchdog circuit, consider the following code:

```
WDBASE% = &H300              'Set watchdog base address to hex300.
OUT WDBASE% + 3, &H90        'Set counter 2 to mode 0,
                             'Read/Load Least Sig. Byte,
                             'Mode 0, binary.
OUT WDBASE +2, 100           'Load Counter 2 Low Byte 100*4.44mSec.
COMBASE% = &H3F8             'Set serial commun'n base address as COM1
MCR% = INP(COMBASE%+4)       'Read modem control register at COMBASE + 4.
OUT COMBASE%+4,MCR% OR 4     'Enable watchdog controlled by bit 2 of modem  control
                             register without changing remaining bits.
```

Before the timeout expires, counter 2 must be reloaded:

```
OUT WDBASE + 2, 100          'Reload counter 2 low byte 100*4.44 mSec.
```

Temperature Alarm

To test if the internal computer temperature exceeds the preset level, read bit 0 at the Temperature Alarm register (Watchdog base address + 4). Bit 0 will be a "0" if temperature is normal and "1" if temperature is excessive. Bits 1 through 7 of this register are meaningless.

Serial Output

The serial communications port has its own base address. If that base address is set as COM1 or COM2, simply follow standard DOS procedures. If serial communications port is NOT set as COM1 or COM2, follow the NS16550 chip (ACE) specification.

The following code sample is in BASIC and demonstrates the recommended steps to initialize the NS16550 for normal operation. This sample assumes a base address of 3F8 and the device will be setup for 9600 baud with an 8-bit, no-parity format. The assumed clock frequency is 1.8432 MHz and, thus, a divisor of 12 is required. (The divisor is determined by dividing the clock frequency by 16 then by the baud rate).

```
OUT &H3FC, &H10        'Put into loopback.
OUT &H3FB, &H80        'Select divisor latch.
OUT &H3F8, 12          'Lower half of 9600 baud divisor.
OUT &H3F9, 0           'Upper half of 9600 baud divisor.
OUT &H3F8, 3           'Deselect divisor latch, set 8 bits/1 stop/no parity
TMP = INP(&H3F8)       'Read input port.
FOR TMP = 1 TO 2       'Wait for at least two character times.
NEXT
TMP = INP(H3F8)        'Read input port a second time.
OUT &H3FC, 1           'Take out of loopback; set "Dir".
```

The following code is a PASCAL version of the preceding BASIC routine.

```
Const ace = $3F8;
var i:integer;
port[ACE+4] := $10;         (put in loopback)
port[ACE+3] := $80;         (select divisor latch)
port[ACE+0] := 12;          (divisor lower byte)
port[ACE+1] := 0;           (divisor upper byte)
port[ACE+3] := 3;           (deselect divisor, set 8 bits/1 stop)
i :=port[ACE];              (read input port)
delay(2);                   (wait two character times)
i :=port[ACE];              (read input port a second time)
port[ACE+4] := 1;           (take out of loopback and set DTR)
```

When the above steps are completed, the chip is ready to communicate.

Sample Programs

There are sample programs provided with the WDG-SIO card in C, Pascal, QuickBASIC, and several Windows languages. DOS samples are located in the DOS directory and Windows samples are located in the WIN32 directory.

Initialization

Initializing the chip requires knowledge of the UART's register set. The first step is to set the baud rate divisor. You do this by first setting the DLAB (Divisor Latch Access Bit) high. This bit is located at Base Address +3, Bit 7. In C, the call would look like:

    outportb(BASEADDR +3,0x80);

You then load the divisor into Base Address +0 (lower byte) and Base Address +1 (higher byte). The following equation defines the relationship between baud rate and divisor:

    desired baud rate = (crystal frequency) / (16   divisor)

The standard crystal frequency is 1.8432 MHz. Commonly used divisors are: 12 for 9600 baud, 48 for 2400 baud, and 96 for 1200 baud. In C, the code to set the chip to 9600 baud is:

    outportb(BASEADDR, 0x0C);
    outportb(BASEADDR +1,0);

The second step when initializing the UART is to set the Line Control Register at Base Address +3. This register defines word length, stop bits, parity, and the DLAB.

Bits 0 and 1 control word length and allow word lengths from five to eight bits. Bit settings are extracted by subtracting 5 from the desired word length.

Bit 2 determines the number of stop bits. If Bit 2 is set to 0, there will be one stop bit. If Bit 2 is set to 1, there will be two stop bits.

Bits 3 through 6 control parity and break enable. They are not commonly used for communications and should be set to 0s.

Bit 7 is the DLAB. It must be set to 0 after the divisor is loaded or else there will be no communications.

In C, the command to set the UART for an eight-bit word, no parity, one stop is:

    outportb(BASEADDR +3, 0x03);

The third initialization step is to set the MODEM control register at Base Address +4. This register controls functions on some cards. Bit 1 is the Request to Send (RTS) control bit. This bit should be left low until transmission time. Bits 2 and 3 are user-designated outputs. Bit 2 may be ignored on this card. Bit 3 is used to enable interrupts and should be set high if an interrupt-driven receiver is to be used.

The final initialization step is to flush the receiver buffers. You do this with two Reads from the receiver buffer at Base Address +0. When this is done, the UART is ready to use.

Reception

Reception can be handled two ways: polling and interrupt-driven. When polling, reception is accomplished by constantly reading the Line Status Register at Base Address +5. Bit 0 of this register is set high whenever data are available to be read from the chip. A simple polling loop must continuously check this bit and read in data when it becomes available. Polling is not effective at high data rates because the program cannot do anything else when it is polling or data could be missed. The following is a code fragment that implements a polling loop and uses a value of zero as an end-of-transmission marker:

```
do
{
while (!(inportb(BASEADDR +5) & 1));/*Wait until data ready*/
data[i++]=inportb(BASEADDR);
}
while (data[i]!=0;/*Reads the line until null character rec'd*/
```

Interrupt-driven communications should be used whenever possible and is required for high data rates. Writing an interrupt-driven receiver is not much more complex than writing a polled receiver. However, care should be taken when installing or removing your interrupt handler because there is a danger of writing the wrong interrupt, or disabling the wrong interrupt, or even turning interrupts off for too long a period.

The handler must first read the Interrupt Identification Register at Base Address +2. If the interrupt is for Received Data Available, the handler then reads the data. If no interrupt is pending, control exits the routine. A sample handler in C is as follows:

```
do
{
readback = inportb(BASEADDR +2);
if(readback & 4) //*Readback will be set to 4 if data are available*/
data[i++]=inportb(BASEADDR);
}
while(readback!=1);
outportb(0x20,0x20);/*Write EOI to 8259 Interrupt Controller*/
return;
```

Transmission

RS485 transmission is simple to implement. First, the RTS line should be set high by writing a 1 to Bit 1 of the modem control register at Base Address +4. The RTS line is used to toggle the transceiver from receive mode to transmit mode and vice versa. It is not carried out on the line in RS485 and not used for handshaking.

Similarly, the CTS line is not used in RS485 and should either be enabled by installing the CTS jumper or installing a jumper in the I/O connector as described in the Option Selection section of this manual.

After the above is done, the card is ready to send data. To transmit a string of data, the transmitter must check Bit 5 of the Line Status Register at Base Address +5. That bit is the transmitter-holding-register-empty flag. If it is high, the transmitter has sent the data. The process of checking the bit until it goes high followed by a write is repeated until no data remains. After all data has been transmitted, the RTS bit should be reset by writing a 0 to Bit 1 of the MODEM control register.

The following C code fragment demonstrates this process:

```
outportb(BASEADDR +4, inportb(BASEADDR +4) 0x02;  /*Set RTS bit without
    altering states of other
    bits*/
while(*data)/*While there is data to send*/
{
while(!(inportb(BASEADDR +5)&0x20));/*Wait until transmitter is empty*/
outportb(BASEADDR,*data);
data++;
}
outportb(BASEADDR +4, inportb(BASEADDR +4)&0xFD;
/*Reset RTS bit without altering states of other bits*/
```

Chapter 6: Connector Pin Assignments

The popular 25-pin D-subminiature connector is used to interface to communication lines. The connector is equipped with #4-40 threaded screws to provide strain relief. The mating connector is AMP type 747304-2 or equivalent. If Option C is included on the card, connections to Counter/Timers 0 and 1 are via a 9-pin D-subminiature connector. The mating connector is AMP type 747304-4 or equivalent.

Connector J2	
Pin	**Assignment**
1	
2	
3	
4	Request to Send (RTS)
5	Clear to Send (CTS)
6	
7	Signal Ground (GND)
8	
9	
10	
11	
12	Receive Line + (RX+)
13	Receive Line - (RX-)
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	Transmit Line + (TX+)
25	Transmit Line - (TX-)

Connector J1	
Pin	**Assignment**
1	Counter 0 Output
2	Counter Output Common
3	Watchdog Out
4	Cntr 1 Opto/Rly Out
5	Cntr 0 Opto/Rly Out
6	Counter 1 Out
7	Ext. Clock In
8	Counter 0 Gate Input
9	Counter 1 Inverted Out

Table 6-1: Connector Pin Assignments

Note

For Simplex, Half-Duplex, and Full-Duplex communications, see the Option Selection section of this manual for pin connection information.

Appendix A: Application Considerations

Introduction

Working with RS422 and RS485 devices is not much different from working with standard RS232 serial devices and these two standards overcome deficiencies in the RS232 standard. First, the cable length between two RS232 devices must be short; less than 50 feet at 9600 baud. Second, many RS232 errors are the result of noise induced on the cables. The RS422 standard permits cable lengths up to 5000 feet and, because it operates in the differential mode, it is more immune to induced noise.

Connections between two RS422 devices (with CTS ignored) should be as follows:

Device #1		Device #2	
Signal	Pin No.	Signal	Pin No.
Gnd	7	Gnd	7
TX$^+$	24	RX$^+$	12
TX$^-$	25	RX$^-$	13
RX$^+$	12	TX$^+$	24
RX$^-$	13	TX$^-$	25

Table A-1: Connections Between Two RS422 Devices

A third deficiency of RS232 is that more than two devices cannot share the same cable. This is also true for RS422 but RS485 offers all the benefits of RS422 plus allows up to 32 devices to share the same twisted pairs. An exception to the foregoing is that multiple RS422 devices can share a single cable if only one will talk and the others will all receive.

Balanced Differential Signals

The reason that RS422 and RS485 devices can drive longer lines with more noise immunity than RS232 devices is that a balanced differential drive method is used. In a balanced differential system, the voltage produced by the driver appears across a pair of wires. A balanced line driver will produce a differential voltage from ± 2 to ± 6 volts across its output terminals. A balanced line driver can also have an input "enable" signal that connects the driver to its output terminals. If the "enable signal is OFF, the driver is disconnected from the transmission line. This disconnected or disabled condition is usually referred to as the "tristate" condition and represents a high impedance. RS485 drivers must have this control capability. RS422 drivers may have this control but it is not always required.

A balanced differential line receiver senses the voltage state of the transmission line across the two signal input lines. If the differential input voltage is greater than +200 mV, the receiver will provide a specific logic state on its output. If the differential voltage input is less than -200 mV, the receiver will provide the opposite logic state on its output. A maximum operating voltage range is from +6V to -6V allows for voltage attenuation that can occur on long transmission cables.

A maximum common mode voltage rating of ±7V provides good noise immunity from voltages induced on the twisted pair lines. The signal ground line connection is necessary in order to keep the common mode voltage within that range. The circuit may operate without the ground connection but may not be reliable.

Parameter	Conditions	Min.	Max.
Driver Output Voltage (unloaded)		4V	6V
		-4V	-6V
Driver Output Voltage (loaded)	LD and LDGND	2V	
	jumpers in	-2V	
Driver Output Resistance			50Ω
Driver Output Short-Circuit Current			±150 mA
Driver Output Rise Time			10% unit interval
Receiver Sensitivity			±200 mV
Receiver Common Mode Voltage Range			±7V
Receiver Input Resistance			4KΩ

Table A-2: RS422 Specification Summary

To prevent signal reflections in the cable and to improve noise rejection in both the RS422 and RS485 mode, the receiver end of the cable should be terminated with a resistance equal to the characteristic impedance of the cable. (An exception to this is the case where the line is driven by an RS422 driver that is never "tristated" or disconnected from the line. In this case, the driver provides a low internal impedance that terminates the line at that end.)

Note

You do not have to add a terminator resistor to your cables when you use the WDG-SIO card. Termination resistors for the RX+ and RX- lines are provided on the card and are placed in the circuit when you install the LD and LDGND jumpers. Moreover, installing the +BIAS and -BIAS jumpers properly biases these lines. (See the Option Selection section of this manual.)

RS485 Data Transmission

The RS485 Standard allows a balanced transmission line to be shared in a party-line mode. As many as 32 driver/receiver pairs can share a two-wire party line network. Many characteristics of the drivers and receivers are the same as in the RS422 Standard. One difference is that the common mode voltage limit is extended and is +12V to -7V. Since any driver can be disconnected (or tristated) from the line, it must withstand this common mode voltage range while in the tristate condition.

The following illustration shows a typical multidrop or party line network. Note that the transmission line is terminated on both ends of the line but not at drop points in the middle of the line.
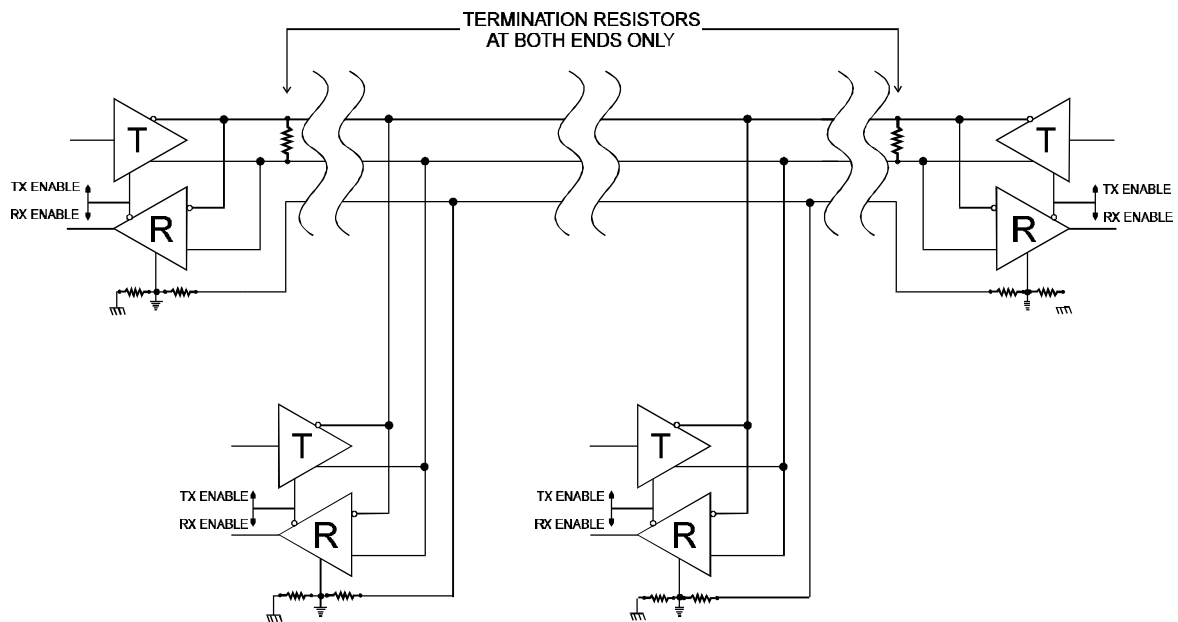
Figure A-1: Typical RS485 Two-Wire Multidrop Network

RS485 Four-Wire Multidrop Network

An RS485 network can also be connected in a four-wire mode. In a four-wire network it's necessary that one node be a master node and all others be slaves. The network is connected so that the master communicates to all slaves and all slaves communicate only with the master. This has advantages in equipment that uses mixed protocol communications. Since the slave nodes never listen to another slave's response to the master, a slave node cannot reply incorrectly.

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: *manuals@accesioproducts.com.*. Please detail any errors you find and include your mailing address so that we can send you any manual updates.